SIMTEC ELECTRONICS

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IM2440D20 Physical memory map

Contents

Introduction

This document shows the physical memory layout of the IM2440D20 which is available in addition to that specified in the Samsung 2440 datasheet.

All memory locations given in this document are physical addresses as seen by the Samsung S3C2440 SOC. Access to these memory addresses may be translated by the bootloader or Operating System (OS) being executed.

The physical memory map decoded by the S3C2440 external memory controller, that is memory mapped I/O which affects external pins, is the first gigabyte of address space.

The S3C2440 SOC has numerous other peripherals which are mapped outside of this first gigabyte and are documented in the Samsung S3C2440 datasheet.

The IM2440D20 module control logic directly buffers nOE, nWE, DQM and D(0..15). In addition it controls the buffering of the lower address lines, A(14..0) and D(31..16).

The gigabyte of external memory mapped space is split into eight 128MB regions. Each region is associated with a Chip Select (CS) numbered from 0 to 7.

Chip Select	Address		Description of Contents
	Start	End	
CS<0>	0x00000000	0x00001000	The "stepping-stone" boot SRAM. The area is not available externally for customer applications.
CS<1> User	0x08000000	0x0C000000	The CS<1> area is split by the on-board IM2440D20 logic into two 64MB regions this lower region, with address line 26 clear, is available for use by customer applications (see IM2440D20 Connector pinouts pin 52).
CS<1> Control	0x0C000000	0x10000000	The CS<1>area is split by the on-board IM2440D20 logic into two 64MB regions. This upper region, with address line 26 set, is used for various control registers.
CS<2>	0x10000000	0x18000000	These areas are available to the user for memory mapped device access. The external chip selects are presented on the IM2440D20 module as pins 54 and 56 respectively (see IM2440D20 Connector pinouts for details).
CS<3>	0x18000000	0x20000000	
CS<4>	0x20000000	0x28000000	These areas are available to the user for memory mapped device access. The external chip selects are presented on the IM2440D20 module as pins 58 and 60 respectively (see IM2440D20 Connector pinouts for details). In addition these areas can have their behaviour altered using the logic's "PCMCIA control" registers.
CS<5>	0x28000000	0x30000000	
CS<6>	0x30000000	0x38000000	These areas are reserved for the systems SDRAM controlled by the S3C2440 internal SDRAM controller.
CS<7>	0x38000000	0x40000000	

PCMCIA

The logic supports generating PCMCIA (or ISA) timings for CS<5> (and CS<4> with logic revisions later than 0xD3) when the PCMCIA system is enabled. This allows for longer cycle times than the default CPU IO system, and for use of the ISA nIOCIS16 signal for proper handling of 8/16 bit accesses.

To configure the timing parameters for the IO or Memory accesses, use the PCMCIA control to set the parameters.

When the PCMCIA controller is enabled, nCS(5) becomes the PCMCIA access region, split into IO, Attribute and Memory space based on A26 and A25.

A26	A25	Offset	Description
0	0	0x00000000	PCMCIA Memory region
1	0	0x04000000	PCMCIA IO region
1	0	0x06000000	PCMCIA Attribute memory

It is up to the external socket logic to decode A26 and A25 into the appropriate PCMCIA control lines.

8bit accesses of 16bit areas

The current behaviour of the CPU, when an IO area is selected to be 16bit and an 8bit access happens is to use D(15..8) when accessing addresses with A(0)=1. This can cause problems when an 8bit peripheral is mapped 1:1 in an 16bit area. It is recommended, if possible, that such peripherals have their lowest address line placed on A1 to avoid this issue.

The IM2440D20 logic provides an 8/16 bit fix (ID register 2) which allows nIOCIS16 to be sampled during

The IM2440D20 logic allows the nIOCIS16 signal to be sampled during an access and the data steered to the correct byte lanes. Unlike the PCMCIA system this does not do an 16 bit to two 8 bit conversion. This is controlled using the global enable in control register 1 or using the individual enables in control register 3.

CS<0> - Internal SRAM

Physical location: 0x00000000 - 0x00001000

The IM2440D20 is configured to boot from NAND flash. When using this mode of operation the S3C2440 SOC maps its internal 4k boot SRAM into CS0. The SRAM is filled with the first 4K of the NAND memory (usually containing the Simtec Initial Program Loader (IPL)) from which the processor starts its execution.

CS<1> - User space

Physical location: 0x08000000 - 0x0C000000

This part of CS1 with A26 clear is available for user applications.

CS<1> - Control Registers

Physical location: 0x0C000000 - 0x10000000

The IM2440D20 has 8 registers for status and control provided by integrated programmable logic. These registers are in CS<1> and are decoded when address bit 26 is set. Any external logic must ignore any accesses to this area. The IM2440D20 logic does not gate nWE or nOE when the internal registers are selected.

An ID register uniquely identifies the control logic version. There have been two released revisions of the logic. The first edition (0xD3) is for small page NAND devices and (0xD5) for large page NAND. The availability and contents of some registers have changed between these two editions and are detailed as appropriate.

Register	Access		Address bits				Offset	Physical address
	Read	Write	A26	A25	A24	A23		
Control 0	R	W	1	0	0	0	0x04000000	0x0C000000
Control 1	R	W	1	0	0	1	0x04800000	0x0C800000
Control 2[1]	R	W	1	0	1	0	0x05000000	0x0D000000
Control 3[1]	R	W	1	0	1	1	0x05800000	0x0D800000
Control 0	R		1	1	0	0	0x06000000	0x0E000000
ID register 2	R		1	1	0	1	0x06800000	0x0E800000
PCMCIA control		W	1	1	1	0	0x07000000	0x0F000000
ID register 1	R		1	1	1	1	0x07800000	0x0F800000

[1] These registers are only available on logic revisions later than 0xD3

Control 0

Physical location: CS<1> + 0x04000000 = 0x0C000000

This is a general purpose control register for accessing several miscellaneous signals. The register is available in all versions of the logic however bits 4 and 5 behaviour is altered.

There is no provision in this register for determining the NAND page size from which the system booted. The information is available from the S3c2440 NAND flash controller which retains the information after a reset.

Bit	Name	Access		States	
		Read	Write		
1,0	NAND flash selection	R	W	00	Internal flash nFCE(0)
				01	Internal flash nFCE(1)
				10	External flash nFCE
				11	External flash nFCE
2	8/16 bit via nIOCIS16	R	W[1]	0	disabled (default)
				1	enabled
3	NAND boot configuration	R		0	external flash, d(1..0) = 10
				1	internal flash, d(1..0) = 00
4	PCMCIA global enable[2]	R		0	disabled
				1	either nCS(5..4) enabled
5	Address buffers permanently enabled	R	W[3]	0	Address buffers enabled on access
				1	Address buffers enabled all the time
6	PCMCIA global nWAIT enable	R		0	PCMCIA controller ignores nWAIT
				1	PCMCIA controller uses nWAIT

7	PCMCIA global nIOCIS16 disable	R	0	nIOCIS16 is used by PCMCIA controller
			1	nIOCIS16 line to PCMCIA controller always asserted (ncs5)

[1]This bit is read only, but can be modified using bit 0 of Control register 1.

[2]For logic versions later than 0xD3 This bit represents if *either* PCMCIA slot is enabled (chip selects 4 or 5). Logic at version 0xD3 or earlier only supports one PCMCIA slot attached to chip select 5.

[3]For logic versions 0xD3 or earlier this bit cannot be written.

Control 1

At nCS(1) + 0x04800000

Bit	Name	Access	States	
		Read Write		
0	8/16 bit via nIOCIS16	W	0	disabled
			1	enabled

This register is write only, to read back the current setting, use Bit 2 of control register 0.

Control 2

At nCS(1) + 0x05000000

This register is only available on logic revisions after 0xD3.

Bit 1 allows the buffers for nOE, nWE, D(15..0) and DQM to be tristated when PWR_EN from the CPU is low, which is when the CPU is either off or in suspend.

Bit 1 may become ro and forced '1' if the global tristate from the XO's PWR_EN pin is used to power the device down over sleep.

Bit	Name	Access	States
		Read Write	

0	NAND flash write-protect signal	R	W[1]	0	NAND flash is write protected
				1	NAND flash is not write protected
1	PWR_EN buffer control	R	W[2]	0	PWR_EN does not tristate buffers
				1	PWR_EN is allowed to tristate buffers
2	PCMCIA nCS(4) enable status	R		0	Disabled
				1	Enabled
3	PCMCIA nCS(5) enable status	R		0	Disabled
				1	Enabled
4	PCMCIA nCS(4) nWAIT enable status	R		0	Disabled
				1	Enabled
5	PCMCIA nCS(5) nWAIT enable status	R		0	Disabled
				1	Enabled
6	PCMCIA nCS(4) nIOCIS16 enable status	R		0	Disabled
				1	Enabled
7	PCMCIA nCS(5) nIOCIS16 enable status	R		0	Disabled
				1	Enabled

[1]To write this bit, bit 2 must also be set. e.g. 0x5 to set and 0x4 to clear.

[2]To write this bit, bit 3 must also be set. e.g. 0xA to set and 0x8 to clear.

Control 3

Physical location: CS<1> + 0x05800000 = 0x0D800000

This register is only available on logic revisions after 0xD3.

This register enables the use of the nIOCIS16 signal to control 8 or 16 bit accesses. The enables are the logical or of these bits and the global enable in the control 0 register.

The enables for CS4 and CS5 are ignored if PCMCIA is enabled.

Bit	Name	Access		States
		Read	Write	
0	Enable nIOCIS16 use for 8/16bit access on CS<1>	R	W	0 Disabled 1 Enabled
1	Enable nIOCIS16 use for 8/16bit access on CS<2>	R	W	0 Disabled 1 Enabled
2	Enable nIOCIS16 use for 8/16bit access on CS<3>	R	W	0 Disabled 1 Enabled
3	Enable nIOCIS16 use for 8/16bit access on CS<4>	R	W	0 Disabled 1 Enabled
4	Enable nIOCIS16 use for 8/16bit access on CS<5>	R	W	0 Disabled 1 Enabled

ID register 2

Physical location: CS<1> + 0x06800000

This will always read 0xEF

PCMCIA control

Physical location: CS<1> + 0x07000000

The register is write-only. The command and data are written together, with the command in d(15..12) and the data in the relevant data bits. For example, to turn the PCMCIA controller on for nCS(5), write 0xD001 to the register, and to turn it of, 0xD000.

The d(11) signal selects CS<5< when clear or CS<4< when set. For logic revisions 0xD3 and prior this bit cannot be set as only a single PCMCIA chip select is supported.

PCMCIA control command					Description
Hex	D15	D14	D13	D12	
0	0	0	0	0	PCMCIA IO setup time in ticks on d(3..0)
1	0	0	0	1	PCMCIA IO assert time in ticks on d(3..0)
2	0	0	1	0	PCMCIA IO hold time in ticks on d(3..0)
4	0	1	0	0	PCMCIA MEM setup time in ticks on d(3..0)
5	0	0	0	0	PCMCIA MEM assert time in ticks on d(3..0)
6	0	0	0	0	PCMCIA MEM hold time in ticks on d(3..0)
C	1	1	0	0	PCMCIA nWAIT control on d(0) 0 PCMCIA controller ignores nWAIT 1 PCMCIA controller used nWAIT
D	1	1	0	1	PCMCIA enable control on d(0) 0 Disabled 1 Enabled
F	1	1	1	1	PCMCIA nIOCIS control on d(0)

0	nIOCIS16 is used by PCMCIA controller
1	nIOCIS16 is ignore by PCMCIA controller

The timing units are in ticks of approximately 83ns. The setup time is the period from the nCS going low to the data-strobe (nOE/nWE), followed by the assert time for the data strobe and then the hold time controls the period until nCS goes high again.

The setup time for the address line is controlled by the CPU timing registers.

```
nCS             ---|_____________________________|------
nOE/nWE         -------------|___________|---------------

                   |< setup >|< assert >|< hold >|
```

If the PCMCIA controller is configured to sample nIOCIS16, then this signal is used to check for 8 or 16bit registers. If an 16bit access is attempted to an 8bit register when this is enabled, then the cycle will be split into two 8bit accesses.

```
nCS     ---|_____________________________________________________________|--
A0      ___________________________________|--------------------------------
nOE/nWE -------------|___________|------------------|___________|-----------

           |< setup >|< assert >|< hold >|< setup >|< assert >|< hold >|
```

Note, there is no time between the end of the hold and the start of the next setup. A0 changes as soon after the end of the first hold period as possible by the logic.

The nOE/nWE cycles can be stretched by nWAIT if configured. nWAIT must be stable one tick before the end of the cycle to be detected.

ID register 1

Physical location: CS<1> + 0x07800000

For the current IM2440D20 this register will return either 0xD3 or 0xD5.

Bit	Name	Access		Value
		Read	Write	
0..2	Logic revision number	R	W	3 Small page NAND modules 5 Large page NAND modules
3..7	Logic product identifier	R	W	0x1A for the IM2440D20 module

CS<2>

Physical location: 0x10000000 - 0x18000000

Application specific memory mapped external peripheral space.

CS<3>

Physical location: 0x18000000 - 0x20000000

Application specific memory mapped external peripheral space.

CS<4>

Physical location: 0x20000000 - 0x28000000

Application specific memory mapped external peripheral space.

This area can be configured for PCMCIA accesses.

CS<5>

Physical location: 0x28000000 - 0x30000000

Application specific memory mapped external peripheral space.

This area can be configured for PCMCIA accesses.

CS<6>

Physical location: 0x30000000 - 0x38000000

SDRAM bank 1

CS<7>

Physical location: 0x38000000 - 0x40000000

SDRAM bank 2

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