SIMTEC ELECTRONICS

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EB675001DIP Connector and link pinouts

Contents

- Introduction
- Dip switches
- 9 way serial
- Main dip connections
- JTAG header

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Introduction

This document shows the pinouts for the EB675001DIP. Several Special Function pins exist which may be changed to simple GPIO if the special function is not required. All I/O pins are protected by level shifting devices allowing full 5V tolerant operation, even direct interfacing with classic 74 series logic (care should be taken with some logic families because the output level from the module will be 3.3V).

Because this module has a user programmable CPLD the I/O pins associated with this device can have almost any function as configured by the uploaded firmware. To accommodate this the *raw* CPLD pin names are presented here e.g. CPLD_PIN55 these correspond to the names in the Xilinx datasheet, if a new CPLD design is being created it is *strongly* recommended that the template project provided by Simtec be used this will perform the correct pin name mapping and the pins will be known by their DIP connector names e.g. CPLD_PIN55 would be D20.

23bits of buffered CPU address lines are available,labelled SA<1> to SA<23> to avoid naming confusion with the main DIP pinouts A1 to A30. The buffer enable is controlled by the user CPLD_PIN28 (active low). These lines are buffered with "Bus Hold" logic this feature holds these lines at their last valid logic state when the drivers goes to high-impedance, thus

eliminating external pull-up/down resistors. The SA<0> line is typically generated by the user CPLD on pin CPLD_PIN54 (D29), this allows the CPLD to be used to control byte lane steering.

The serial port lines are available either as unbuffered LVTTL on B18 to B25 or as fully buffered RS232 compatible signals on pins A26 to B29. The RS232 buffer enable is controlled either by use of the external pin SERIAL_EN (which is normally pulled high) or Switch 5. These signals *only* appear on one set of output pins at any one time, the unbuffered lines may be used as GPIO from the CPU if RS232 is not required. Although the B18 to B25 signals are unbuffered they are still level translated and as such are 5V tolerant, indeed the signal outputs are inhibited by the level converter when SERIAL_EN is high.

The IRQ0 signal on pin A13 is connected to the Davicom Ethernet controller. If the Ethernet is not fitted this signal may be used as a normal interrupt input, otherwise care must be taken about the shared nature. The current uCLinux network driver does not support shared operation and fails to operate properly symptoms of this are a large number of overrun events from the network controller and inability to receive data.

Care should be taken with D13 as it has a 10KΩ pull up resistor attached internally.

Dip switches

There is a set of eight switches to control some specific boot time features, usually only switches 1-4 are fitted.

These switches connect normally pulled high lines to ground and hence produce inverted logic i.e. turning the switch *on* sets the signal to 0

The CPU boot mode is described in the OKI ML675001 users manual, these settings are outlined here for completeness.

ML675001 boot modes

Switch 3 (Boot 0)	Switch 4 (Boot 1)	Description
Off	Off	Built in boot ROM
Off	On	External Flash
On	Off	Built in boot ROM
On	On	External Flash

EB675001DIP SW1 dip switches

Switch	Function	Description
1	Rom Swap	Inverts top address line on external ROM (Flash)
2	Rom/Ram select	Selects boot source between external ROM(Flash) and optional SRAM
3	Boot 0	Selects CPU boot operation
4	Boot 1	

Switch	Function	Description
5	Serial enable	Controls serial buffering see Introduction to serial for details
6	Backup battery selection	Selects source for RTC power (usually omitted as onboard battery is not fitted)
7	Clock mode 0	CPU clock source selection not fitted (usually controlled by LK4 and LK5)
8	Clock mode 1	

9 way serial connector

9 way serial connector pinouts

Pin	Signal	Description
1	DCD	Buffered RS232 level UART DCD signal [1]
2	RX	Buffered RS232 level UART RX signal [1]
3	TX	Buffered RS232 level UART TX signal [1]
4	DTR	Buffered RS232 level UART DTR signal [1]
5	GND	Buffered RS232 level UART GND signal [1]
6	DSR	Buffered RS232 level UART DSR signal [1]
7	RTS	Buffered RS232 level UART RTS signal [1]
8	CTS	Buffered RS232 level UART CTS signal [1]
9	RI	Buffered RS232 level UART RI signal [1]

Note 1: These signals are identical to the ones brought out on A26 through B29. The enable for this signal is controlled by SERIAL_EN line and will only be available if that line is *high*.

Main DIP connections

Physical Layout

The main connections to the module are four rows of standard pitch (0.1 inch) pins. There are thirty pins on each row two rows on each side of the module. A pair of DIN 4139 sockets can be used to connect the module to a baseboard as an alternative to soldering the pins directly.

EB675001DIP DIP pinouts physical layout

Row	Col A	Col B	Col C	Col D
1	VIN	GND	3.3V	GND
2	GND	3.3V	GND	EXT_BAT
3	CPLD_PIN94	CPLD_PIN93	CPLD_PIN92	CPLD_PIN91
4	CPLD_PIN96	CPLD_PIN95	CPLD_PIN89	CPLD_PIN90
5	CPLD_PIN01	CPLD_PIN97	CPLD_PIN86	CPLD_PIN87
6	CPLD_PIN04	CPLD_PIN03	CPLD_PIN82	CPLD_PIN85
7	CPLD_PIN08	CPLD_PIN06	CPLD_PIN79	CPLD_PIN81
8	RST	PWM1	CPLD_PIN77	CPLD_PIN78
9	FIQ	PWM0	CPLD_PIN74	CPLD_PIN76
10	IRQ3	TC1	CPLD_PIN71	CPLD_PIN72
11	IRQ2	TC0	CPLD_PIN68	CPLD_PIN70
12	IRQ1	DACK1	CPLD_PIN66	CPLD_PIN67
13	IRQ0	DREQ1	CPLD_PIN64	CPLD_PIN65
14	SCL	DACK0	CPLD_PIN61	CPLD_PIN63
15	SDA	DREQ0	SA<23>	CPLD_PIN60
16	SD0	SRXD	SA<22>	CPLD_PIN59
17	SD1	STXD	SA<21>	GND
18	SCK	RI	SA<20>	CPLD_PIN58
19	GND	RTS	SA<19>	CPLD_PIN56
20	ANALOG_3	DTR	SA<18>	CPLD_PIN55
21	ANALOG_2	DCD	SA<17>	SA<8>
22	ANALOG_1	DSR	SA<16>	SA<7>
23	ANALOG_0	CTS	SA<15>	SA<6>
24	ANALOG_GND	TX	SA<14>	SA<5>
			SA<13>	SA<4>

Pin Descriptions

EB675001DIP main pinouts by pin number

Pin	Signal	Description
A1	VIN	4.5 - 15V DC power supply
A2	GND	Power ground
A3	CPLD_PIN94	Xilinx XC9572XL I/O Pin 94
A4	CPLD_PIN96	Xilinx XC9572XL I/O Pin 96
A5	CPLD_PIN01	Xilinx XC9572XL I/O Pin 1
A6	CPLD_PIN04	Xilinx XC9572XL I/O Pin 4
A7	CPLD_PIN08	Xilinx XC9572XL I/O Pin 8
A8	RST	Inverted module reset *output*
A9	FIQ	Inverted CPU fast interrupt line
A10	IRQ3	Fourth CPU interrupt line or CPU GPIO 8
A11	IRQ2	Third CPU interrupt line or CPU GPIO 7
A12	IRQ1	Second CPU interrupt line or CPU GPIO 6
A13	IRQ0	First CPU interrupt line or CPU GPIO 5 [5]
A14	SCL	I^2C Serial Clock or CPU GPIO PIOE[4]
A15	SDA	I^2C Serial Data or CPU GPIO PIOE[3]
A16	SDO	Synchronous serial (SSIO) data output
A17	SDI	Synchronous serial (SSIO) data input
A18	SCK	Synchronous serial (SSIO) clock
A19	GND	Signal ground
A20	ANALOG_3	Fourth analog input
A21	ANALOG_2	Third analog input
A22	ANALOG_1	Second analog input
A23	ANALOG_0	First analog input

Pin	Signal	Description
A24	ANALOG_GND	Analog inputs ground reference
A25	VDD_ANALOG	Analog inputs supply reference
A26	RS232_DCD	Buffered RS232 level UART DCD signal 2
A27	RS232_RX	Buffered RS232 level UART RX signal 2
A28	RS232_TX	Buffered RS232 level UART TX signal 2
A29	RS232_DTR	Buffered RS232 level UART DTR signal 2
A30	GND	Serial port ground
B1	GND	DC power supply ground
B2	3.3V	3.3V output from onboard regulator or external 3.3V regulated smoothed supply (see C1).
B3	CPLD_PIN93	Xilinx XC9572XL I/O Pin 93
B4	CPLD_PIN95	Xilinx XC9572XL I/O Pin 95
B5	CPLD_PIN97	Xilinx XC9572XL I/O Pin 97
B6	CPLD_PIN03	Xilinx XC9572XL I/O Pin 3
B7	CPLD_PIN06	Xilinx XC9572XL I/O Pin 6
B8	PWM1	Second Pulse Width Modulator output or CPU GPIO PIOC[1]
B9	PWM0	First Pulse Width Modulator output or CPU GPIO PIOC[0]
B10	TC1	Terminal count for DMA channel 1 or CPU GPIO PIOB[4]
B11	TC0	Terminal count for DMA channel 0 or CPU GPIO PIOB[5]
B12	DACK1	DMA acknowledge/clear for channel 1 or CPU GPIO PIOB[3]
B13	DREQ1	DMA request for channel 1 or CPU GPIO PIOB[2]
B14	DACK0	DMA acknowledge/clear for channel 0 or CPU GPIO PIOB[1]
B15	DREQ0	DMA request for channel 0 or CPU GPIO PIOB[0]

Pin	Signal	Description
B16	SRXD	Simple serial port (SIO) data receive (*not* the UART port) or CPU GPIO PIOB[7]
B17	STXD	Simple serial port (SIO) data transmit or CPU GPIO PIOB[6]
B18	RI	Unbuffered UART RI signal or CPU GPIO PIOA[7] [1]
B19	RTS	Unbuffered UART RTS signal or CPU GPIO PIOA[6] [1]
B20	DTR	Unbuffered UART DTR signal or CPU GPIO PIOA[5] [1]
B21	DCD	Unbuffered UART DCD signal or CPU GPIO PIOA[4] [1]
B22	DSR	Unbuffered UART DSR signal or CPU GPIO PIOA[3] [1]
B23	CTS	Unbuffered UART CTS signal or CPU GPIO PIOA[2] [1]
B24	TX	Unbuffered UART TX signal or CPU GPIO PIOA[1] [1]
B25	RX	Unbuffered UART RX signal or CPU GPIO PIOA[0] [1]
B26	RS232_DSR	Buffered RS232 level UART DSR signal [2]
B27	RS232_RTS	Buffered RS232 level UART RTS signal [2]
B28	RS232_CTS	Buffered RS232 level UART CTS signal [2]
B29	RS232_RI	Buffered RS232 level UART RI signal [2]
B30	SERIAL_EN	RS232 buffer enable (see introduction for more detail)
C1	3.3V	3.3V output from onboard regulator or external 3.3V regulated smoothed supply (see B2).
C2	GND	Supply Ground
C3	CPLD_PIN92	Xilinx XC9572XL I/O Pin 92
C4	CPLD_PIN89	Xilinx XC9572XL I/O Pin 89
C5	CPLD_PIN86	Xilinx XC9572XL I/O Pin 86
C6	CPLD_PIN82	Xilinx XC9572XL I/O Pin 82
C7	CPLD_PIN79	Xilinx XC9572XL I/O Pin 79

Pin	Signal	Description
C8	CPLD_PIN77	Xilinx XC9572XL I/O Pin 77
C9	CPLD_PIN74	Xilinx XC9572XL I/O Pin 74
C10	CPLD_PIN71	Xilinx XC9572XL I/O Pin 71
C11	CPLD_PIN68	Xilinx XC9572XL I/O Pin 68
C12	CPLD_PIN66	Xilinx XC9572XL I/O Pin 66
C13	CPLD_PIN64	Xilinx XC9572XL I/O Pin 64
C14	CPLD_PIN61	Xilinx XC9572XL I/O Pin 61
C15	SA<23>	Buffered CPU address line 4
C16	SA<22>	Buffered CPU address line 4
C17	SA<21>	Buffered CPU address line 4
C18	SA<20>	Buffered CPU address line 4
C19	SA<19>	Buffered CPU address line 4
C20	SA<18>	Buffered CPU address line 4
C21	SA<17>	Buffered CPU address line 4
C22	SA<16>	Buffered CPU address line 4
C23	SA<15>	Buffered CPU address line 4
C24	SA<14>	Buffered CPU address line 4
C25	SA<13>	Buffered CPU address line 4
C26	SA<12>	Buffered CPU address line 4
C27	SA<11>	Buffered CPU address line 4
C28	SA<10>	Buffered CPU address line 4
C29	SA<9>	Buffered CPU address line 4
C30	GND	Signal Ground

Pin	Signal	Description
D1	GND	Signal Ground
D2	EXT_BAT	Supply for the Real Time Clock
D3	CPLD_PIN91	Xilinx XC9572XL I/O Pin 91
D4	CPLD_PIN90	Xilinx XC9572XL I/O Pin 90
D5	CPLD_PIN87	Xilinx XC9572XL I/O Pin 87
D6	CPLD_PIN85	Xilinx XC9572XL I/O Pin 85
D7	CPLD_PIN81	Xilinx XC9572XL I/O Pin 81
D8	CPLD_PIN78	Xilinx XC9572XL I/O Pin 78
D9	CPLD_PIN76	Xilinx XC9572XL I/O Pin 76
D10	CPLD_PIN72	Xilinx XC9572XL I/O Pin 72
D11	CPLD_PIN70	Xilinx XC9572XL I/O Pin 70
D12	CPLD_PIN67	Xilinx XC9572XL I/O Pin 67
D13	CPLD_PIN65	Xilinx XC9572XL I/O Pin 65 [3]
D14	CPLD_PIN63	Xilinx XC9572XL I/O Pin 63
D15	CPLD_PIN60	Xilinx XC9572XL I/O Pin 60
D16	CPLD_PIN59	Xilinx XC9572XL I/O Pin 59
D17	GND	Signal ground
D18	CPLD_PIN58	Xilinx XC9572XL I/O Pin 58
D19	CPLD_PIN56	Xilinx XC9572XL I/O Pin 56
D20	CPLD_PIN55	Xilinx XC9572XL I/O Pin 55
D21	SA<8>	Buffered CPU address line [4]
D22	SA<7>	Buffered CPU address line [4]
D23	SA<6>	Buffered CPU address line [4]
D24	SA<5>	Buffered CPU address line [4]

Pin	Signal	Description
D25	SA<4>	Buffered CPU address line [4]
D26	SA<3>	Buffered CPU address line [4]
D27	SA<2>	Buffered CPU address line [4]
D28	SA<1>	Buffered CPU address line [4]
D29	CPLD_PIN54	Xilinx XC9572XL I/O Pin 54 usually used to generate the bottom bit of the address bus e.g. SA<0>
D30	GND	Signal Ground (Key pin)

Note 1: The enable for this signal is controlled by SERIAL_EN line and will only be available if that line is *low*.

Note 2: These signals are identical to the ones brought out on the 9 way serial connector. The enable for this signal is controlled by SERIAL_EN line and will only be available if that line is *high*.

Note 3: These signals have a 10KΩ pull up resistor.

Note 4: These signals are buffered with bus hold logic and will remain in a given state unless driven.

Note 5: IRQ 0 is shared with the Davicom Ethernet controller and special care must be taken. More details are available in the introduction.

JTAG header

The JTAG header (PL6) provides all the signals necessary to use a JTAG debugger.

EB675001DIP JTAG pinouts by pin number

Pin	Signal	Description
1	3.3v	Supply
2	TRST	TAP reset, reset JTAG TAP controller
3	TDI	TAP data in
4	TMS	Test Mode Select
5	TCLK	TAP clock
6	RCLK	Returned clock
7	TDO	TAP data out

Pin	Signal	Description
8	RST	Inverted system reset
9	GND	Signal ground
10	JSEL	Chain selection

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