SIMTEC ELECTRONICS

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Author:VRS
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EB675001DIP Memory Map

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Introduction

This document explains the layout of the memory in the EB675001DIP module. This module has a reasonably simple memory map mostly derived from the underlying ML675001 (see the OKI ML675001 datasheet section 3).

All addresses are in hexadecimal unless otherwise stated.

Overview

Region	Start Address	End Address	Device
Processor	**00000000**	**3FFFFFFF**	
	00000000	07FFFFFF	Remappable ROM RAM
AMBA High speed BUS (AHB)	**40000000**	**7FFFFFFF**	
	48000000	48001000	Boot ROM
	50000000	58007FFF	Internal SRAM
	78000000	7C000000	Core IO
AMBA Peripheral BUS (APB)	**80000000**	**BFFFFFFF**	
	B0000000	B7FFFFFF	Standard APB I/O
	B8000000	BFFFFFFF	Core APB I/O
External	**C0000000**	**FFFFFFFF**	
	C0000000	C8000000	DRAM
	C8000000	D0000000	ROM
	D0000000	D8000000	SRAM
	F0E00000	F0E40001	Davicom Ethernet
	F8000000	FFFFFFFF	User CPLD region

Processor

The processor region doesn't have any defines sub regions other than the remappable ROM/RAM region at its base.

AMBA High speed BUS

AMBA High speed BUS Core I/O

Start Address	End Address	Description
78000000	7800002F	Interrupt control register
78100000	7817FFFF	External memory and I/O access control register
78180000	78200000	DRAM controller control register
78300000	7BE00000	External I/O access control register
7BE00000	7BF00000	DMA controller control register
7BF00000	7c000000	Expansion control register

AMBA Peripheral BUS

AMBA Peripheral BUS Standard I/O

Start Address	End Address	Description

AMBA Peripheral BUS Core I/O

Start Address	End Address	Description

External Peripherals

External Peripherals

Start Address	End Address	Description
C0000000	C8000000	DRAM
C8000000	CC000000	MCP Flash ROM (not fitted)
CC000000	D0000000	Flash
D0000000	D8000000	SRAM
F0E00000	F0E00001	Davicom Ethernet Address port
F0E40000	F0E40001	Davicom Ethernet Data port
F8000000	FFFFFFFF	User CPLD region

Simtec Electronics

Web:http://www.simtec.co.uk/

Email:info@simtec.co.uk

Simtec Electronics,
Avondale Drive,
Tarleton,
Preston,
Lancs
PR4 6AX
United Kingdom

Tel:+44 (0)1772 812863 Fax:+44 (0)1772 816426