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EB2410ITX User Guide

Simtec Electronics

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EB2410ITX User Guide

Simtec Electronics

by B J Dooks and V R Sanders

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Initial Release.

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EB2410ITX Development Board

About this document. This document describes the Simtec EB2410ITX Development board which provides a flexible development system for both experimentation and integrator solutions.

Intended Audience. This document is aimed at experienced engineers.

Related documents. Some additional documents which may be useful:

Online resources [<http://www.simtec.co.uk/products/EB2410ITX/resources.html>]

Connector and link pinouts. [<http://www.simtec.co.uk/products/EB2410ITX/files/pinlist.html>]

Memory map and control registers. [<http://www.simtec.co.uk/products/EB2410ITX/files/mmap.html>]

Mechanical Drawing [<http://www.simtec.co.uk/products/EB2410ITX/files/EB2410ITX-mechanical.pdf>]

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The document title

The document revision

A clear explanation of your comments and how they apply

Chapter 1. Overview

This chapter describes:

- The kit contents
- Development tools
- Use of the development board
- Handling precautions

1.1. Kit contents

The EB2410ITX is a comprehensive ARM computing platform. The Kit contains:

- The EB2410ITX user guide
- A CD-ROM containing development software and documents relevant to the EB2410ITX
- The EB2410ITX board.

1.1.1. CD-ROM

The CD-ROM contains:

- A copy of all the freely available documentation, including this user guide.
- Datasheets for all major components used
- Embedded Linux distribution
- x86 cross building toolchain for GNU/Linux
- ABLE bootloader

The toolchain contains a GCC compiler, assembler and linker suitable for cross compiling ARM binaries from an x86 machine running GNU/Linux.

1.1.2. EB2410ITX Development board

The EB2410ITX board (gold specification) has the following major components:

- Samsung S3C2410 ARM 920T SOC
- 128MB SDRAM
- 16MBit NOR Flash
- Smartmedia Card Slot
- 8Kbit I2C EEPROM
- 15pin VGA connector
- 4 pin mini-din S-Video connector

- Full I²S audio CODEC with 1.1W integrated amplifier
- Two fully independent 10/100MBit Ethernet controllers
- Two USB full speed host ports
- Parallel port
- 9pin D-sub RS232 port
- 10 Way box header RS232 port
- Additional three RS232 serial ports
- Primary 40 Way standard IDE connector
- Secondary 44way 2mm IDE connector
- MMC/SD expansion
- Parallel port
- JTAG header
- 30 5V tolerant GPIO or special function lines
- ATX power connector

1.2. Development Tools

The development tools provided must be installed and run on a PC with a GNU/Linux Operating system (e.g. Debian, Ubuntu or Redhat distributions). The GCC toolchain provided creates executable binaries that can be run on the EB2410ITX. This toolchain is also required to build the kernel and Embedded Linux. Full details of building Linux are provided on the EB2410ITX resources page.

In order to run the development tools the host PC requires:

- 500MHz or faster processor
- Installed GNU/Linux distribution
- 128MB RAM
- 1GB of hard disk space (3GB if building Embedded Linux)
- CD-ROM Drive

In addition to the development tools, the module usually requires serial communications to access its bootloader and booted system. Most modern PC have serial ports, however increasingly only USB ports are provided, most typical USB->Serial converters appear to work with the EB2410ITX.

1.3. Using the development board

The EB2410ITX is a complete system. With the addition of a suitable power supply and PC the Kit provides everything required to start producing the desired solution. The ABLE bootloader allows a flexible use of the EB2410ITX. ABLE can start Linux images from a variety of sources including the network. In this mode of usage the serial port is used as a console to communicate with the device.

1.4. Handling precautions

This development board is intended for use either within a workshop/laboratory environment or as an integrator solution

within a larger product. Because of this the EB2410ITX board is supplied without an enclosure. The lack of an enclosure means that standard electrostatic control procedures should be used when handling the board. When using the EB2410ITX outside an enclosure the following is recommended:

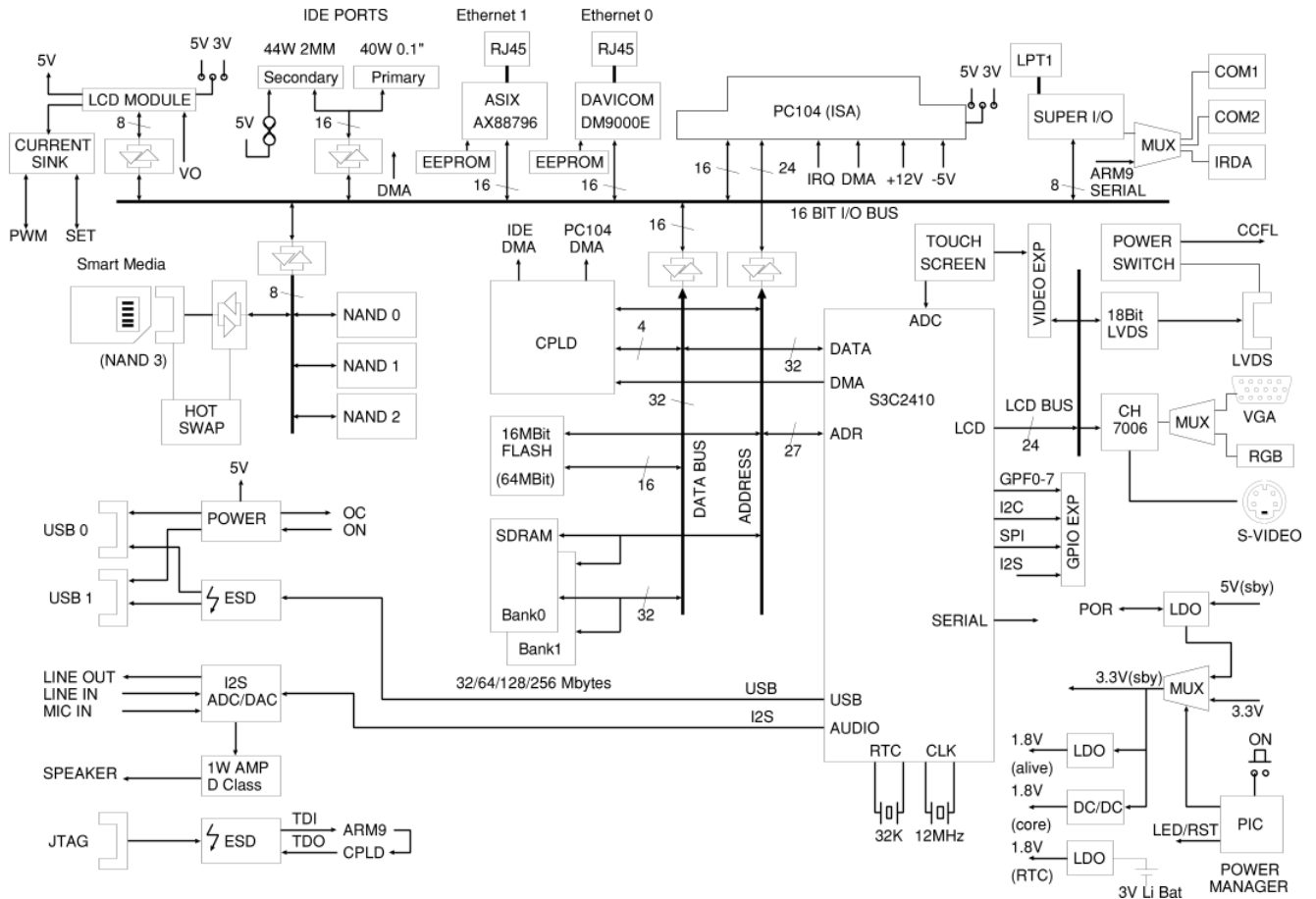
- Only hold the board by the edges
- Always use proper static handling equipment, as a minimum an earth strap

Chapter 2. Hardware Description

2.1. Overview

The EB2410ITX is a complete system that includes a large number of Input/Output facilities. Simtec Electronics provide a number of application notes accessible via the EB2410ITX resources page or on the supplied CD-ROM which demonstrate the use of the board.

Figure 2.1. Detailed block diagram of the EB2410ITX



2.2. Samsung S3C2410 SOC

The S3C2410 is a 272 ball fine pitch Ball Grid Array (BGA) device from Samsung. The large number of peripherals within the device give flexibility to the user and the ability to use numerous I/O solutions without additional controllers. The S3C2410 has a full MMU and high bandwidth memory system allowing a range of standard operating systems to be run. The S3C2410 has a Harvard architecture 16KByte Data/16KByte instruction cache which further improves performance. The power management systems within the SOC allow for very flexible power control and with a typical power usage of 0.3W at 266MHz operating speeds contributes towards the EB2410ITX low overall power consumption.

Simtec provide Debian GNU/Linux as standard which provides a full development environment identical in look and feel to an x86 install of Debian GNU/Linux.

The large number of peripherals and interfaces are summarised as follows:

- ARM920T 32-bit RISC CPU
- 32-bit mode (ARM) and/or 16-bit mode (Thumb)

- Built-in SDRAM external memory controller supports glue-less connectivity to memory.
- External memory controller supporting external NOR flash and SRAM
- Independent NAND memory controller
- 55 internal interrupt sources
- 24 external interrupt sources
- Four DMA channels
- One 16-bit system timer
- Four 16-bit auto reload timers with independent clock settings
- One flexible 16 bit watchdog timer
- 117 GPIO bits
- Eight 10-bit Analog channels
- Three channel UART
- Master mode I²C controller
- MMC/SD controller.
- Two USB full speed host ports.
- Flexible power management including standby and halt operation modes
- Integrated Real Time Clock (RTC).
- Video controller with dedicated DMA controller.

For further details on the S3C2410 please consult the Samsung S3C2410 User manual [<http://www.samsung.com/Products/Semiconductor/SystemLSI/MobileSolutions/MobileASSP/MobileComputing/S3C2410/S3C2410.htm>]

2.3. Serial ports

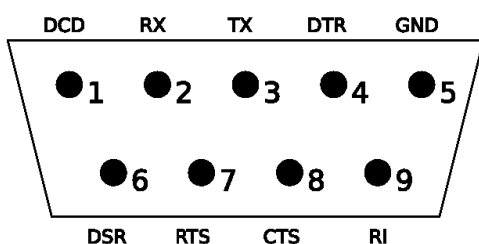
The S3C2410 has three serial ports complete with FIFO. The first port is used as a console port by the bootloader and Linux.

There is an optional super I/O controller which provides an additional two serial ports.

There are two ports which are buffered and level translated to RS232 signal levels. The first is an external 9way D port (PL1) and the second is a ten way box header (PL7).

The ports output through the level converters may be selected from any of the five available sources by using the jumper matrix (LK2 to LK17). For more details on the ports usage and jumper matrix refer to the EB2410ITX Connector and link pinouts [<http://www.simtec.co.uk/products/EB2410ITX/files/pinlist.html>] document.

Figure 2.2. External 9way D Serial connector



2.4. Real Time Clock

The Real Time Clock (RTC) is integrated into the S3C2410. The RTC has a 32KHz crystal attached. The RTC has the capacity to hold the date and time and keep them using a minimum of power, typically 3uA with 1.8V supply. There is also the ability to set alarms which may generate interrupts, this may be used to perform repeating tasks with long intervals without consuming large amounts of power.

2.5. JTAG

The S3C2410 and the system CPLD are connected to a single JTAG chain. The JTAG chain is available from this 0.1inch 20way connector and allows reprogramming of the user CPLD and ICE debugging of the processor. This connector has the standard ARM Multi-ICE pinout so most JTAG debuggers will be compatible.

Figure 2.3. JTAG connector

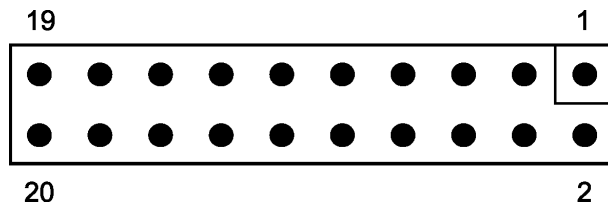


Table 2.1. JTAG connector PL18

Pin	Name	Description
1	3.3V	3.3V supply
2	3.3V	3.3V supply
3	nTRST	Inverted Tap reset
4	GND	Signal Ground
5	TDI	Data In
6	GND	Signal Ground
7	TMS	
8	GND	Signal Ground
9	TCK	
10	GND	Signal Ground
11	RCLK	Return clock, pulled down with 390ohm to ground
12	GND	Signal Ground
13	TDO	Tap data out
14	GND	Signal Ground
15	nSRST	Inverted system reset
16	GND	Signal Ground
17	N/C	Not connected
18	GND	Signal Ground
19	N/C	Not connected
20	GND	Signal Ground

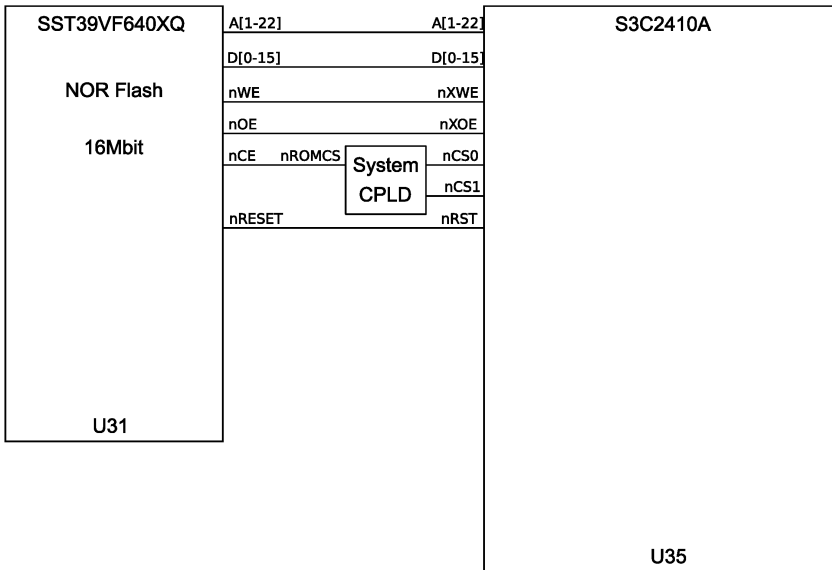
The JTAG chain on the EB2410ITX is connected to the S3C2410 and system CPLD. Because of this care should be taken to ensure the system CPLD is placed in bypass. BSDL files are available from Samsung for the S3C2410 and Xilinx for the CPLD device.

2.6. Memory

2.6.1. NOR boot flash

The EB2410ITX has provision for a single NOR flash device. This device typically contains the bootloader and optionally a Linux image to boot, though it can contain anything the user requires. The flash is implemented as a single sixteen bit wide device, which is selected by use of the nROMCS chip select from the system CPLD, nROMCS is derived from nCS<0> and nCS<1> from the S3C2410. This memory appears read only in chip select 0 (0x00000000 to 0x01FFFFFF) and read/write in chip select 1 (0x0C000000 to 0x0DFFFFFF) of the S3C2410 physical memory map.

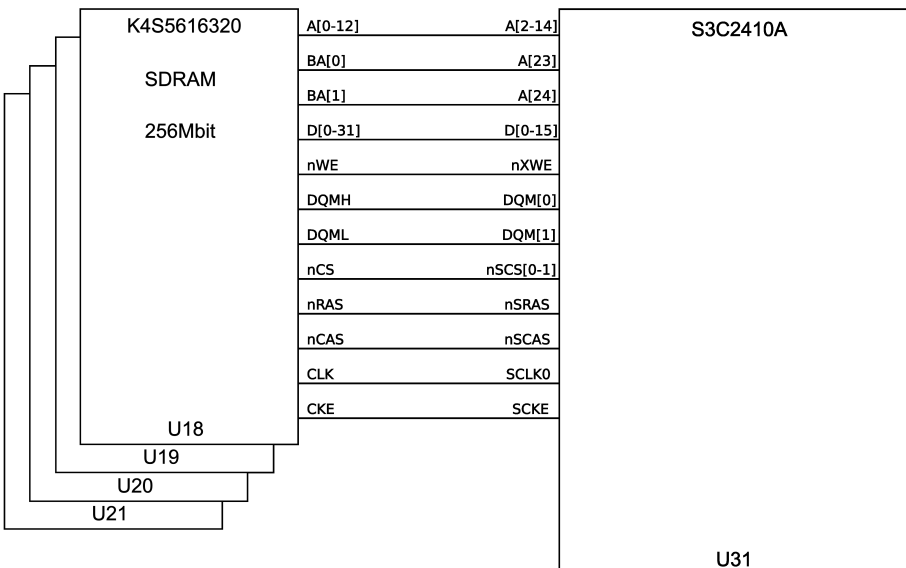
Figure 2.4. NOR flash to S3C2410 attachment



2.6.2. SDRAM

The EB2410ITX has provision for four SDRAM devices with either the default 256MBit capacity or a 512MBit capacity. This memory, where fitted, is accessed using the S3C2410 SDRAM controller and appears in banks six and seven of its physical memory map (0x30000000 and 0x38000000).

Figure 2.5. SDRAM to S3C2410 attachment



2.6.3. EEPROM

There is provision for a single EEPROM connected via the I²C bus. All specification boards have an 8KBit (1KB) device fitted as standard but up to 256KBit can be accommodated. The device is typically used to hold the non volatile settings in the ABL boot-loader.

2.7. Super IO controller

The EB2410ITX has provision for an additional super IO controller which provides two additional 16550 type serial ports, a full function parallel port and a full IRDA interface.

2.8. Power Supply

The board may be powered either by the standard 20 way ATX type Molex connector or the 20 way SIL 0.1inch auxiliary power connector.

The ATX power supply must be suitable for the EB2410ITX. A supply rated for operation of 80W or less is recommended as higher rated supplies are not stable under the very small power draw of the board.

Figure 2.6. 20 pin MOLEX 39-29-9202 ATX power connector

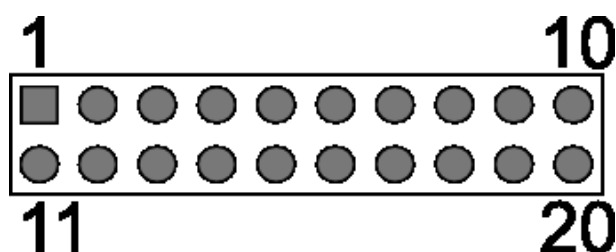


Table 2.2. ATX power connector pinouts PL23

Pin	Name	Description
1	3.3V	3.3 Volt supply
2	3.3V	3.3 Volt supply
3	GND	Power ground
4	5V	5 Volt supply
5	GND	Power ground
6	5V	5 Volt supply
7	GND	Power ground
8	DC_OK	DC supply is ready
9	5V_SBY	5V Standby
10	12V	12 Volt supply
11	3.3V	3.3 Volt supply
12	-12V	12 Volt negative supply
13	GND	Power ground
14	PSU_EN	Power supply enable
15	GND	Power ground
16	GND	Power ground
17	GND	Power ground
18	-5V	Negative 5 Volt supply
19	5V	5 Volt supply

Pin	Name	Description
20	5V	5 Volt supply

Figure 2.7. 20 pin auxiliary SIL power connector

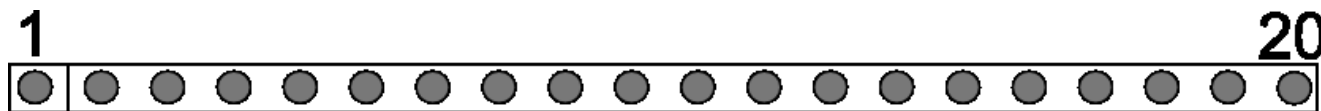


Table 2.3. SIL power connector pinouts PL24

Pin	Name	Description
1	3.3V	3.3 Volt supply
2	3.3V	3.3 Volt supply
3	GND	Power ground
4	GND	Power ground
5	5V	5 Volt supply
6	5V	5 Volt supply
7	5V_SBY	5 Volt standby
8	ALIVE	Supply alive
9	12V	12 Volt supply
10	GND	Power Ground
11	GND	Power Ground
12	-12V	12 Volt negative supply
13	-5V	5 Volt negative supply
14	GND	Power supply ground
15	PWM	Enable PWM supply
16	5V_EN	5 volt supply enable
17	3V_EN	3 volt supply enable
18	PSU_ON	Supply on switch
19	PG	Power Good
20	IO/VIN	ADC Vin for supply monitoring

Some typical power usages are presented here in Table 2.4, “Typical power usage”. A fully specified platinum board with CPU clocked at 202MHz, memory bus at 101MHz, 256MB of SDRAM and all options fitted was used to profile the worst case power usage with no USB peripherals fitted.

Table 2.4. Typical power usage

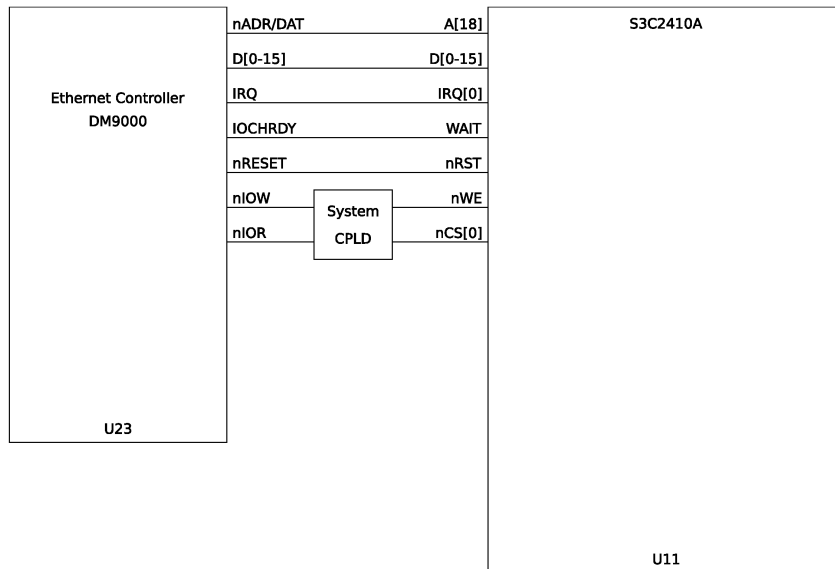
Tested Configuration	Current From 3.3V	Current From 5V	Total power usage
serial + both network ports + video	500mA	167mA	2.49W
serial + one network port + video	435mA	167mA	2.27W
serial + both network ports	425mA	56mA	1.68W
serial + one network port	360mA	56mA	1.47W
serial only	275mA	56mA	1.19W

All figures are subject to a 1% measurement accuracy and are for guidance purposes only.

2.9. DM9000 Network controller

The DM9000 network controller provides 100Mbit Ethernet connectivity to the system. It is decoded into the CS0 address space by the system CPLD as it uses the WAIT line to extend I/O cycles as necessary.

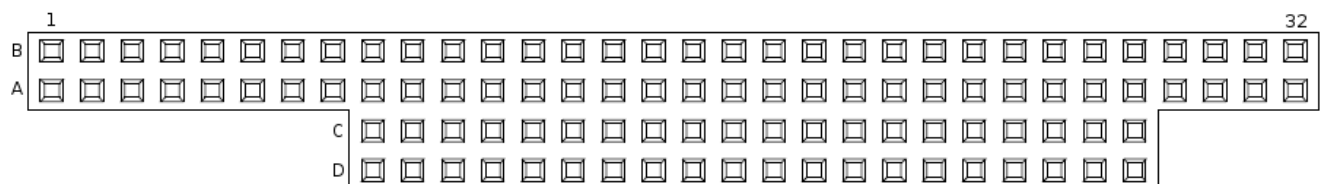
Figure 2.8. DM9000 to S3C2410 attachment



2.10. PC104 expansion connectors

The EB2410ITX has an industry standard 16 bit PC104 socket.

Figure 2.9. PC104 Expansion connector



For full details the EB2410ITX Connector and link pinouts [<http://www.simtec.co.uk/products/EB2410ITX/files/pinlist.html>] document should be consulted, this contains additional information and comments relevant to using this product.

Table 2.5. PC104 expansion connector PL13

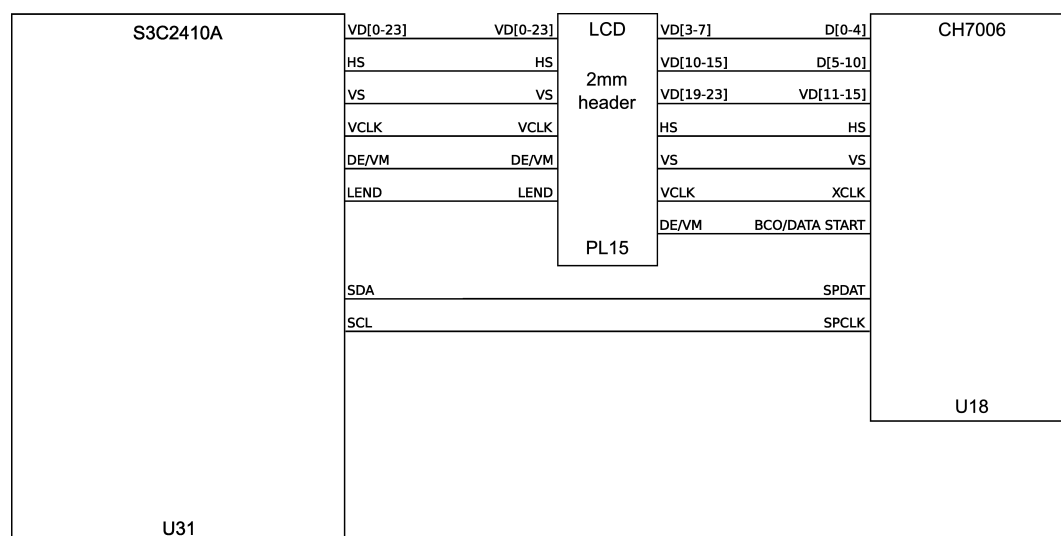
Pin	Row D	Row C	Pin	Row A	Row B
			1	IOCHK	GND
			2	SD7	RESET
			3	SD6	+5V
			4	SD5	IRQ9
			5	SD4	-5V
			6	SD3	DRQ2
			7	SD2	-12V
			8	SD1	SRDY
0	GND	GND	9	SD0	+12V

Pin	Row D	Row C	Pin	Row A	Row B
1	MEMCS16	SBHE	10	IOCHRDY	KEY
2	IOCS16	LA23	11	AEN	SMEMW
3	IRQ10	LA22	12	SA19	SMEMR
4	IRQ11	LA21	13	SA18	IOW
5	IRQ12	LA20	14	SA17	IOR
6	IRQ15	LA19	15	SA16	DACK3
7	IRQ14	LA18	16	SA15	DRQ3
8	DACK0	LA17	17	SA14	DACK1
9	DRQ0	MEMR	18	SA13	DRQ1
10	DACK5	MEMW	19	SA12	REFRESH
11	DRQ5	SD8	20	SA11	BCLK
12	DACK6	SD9	21	SA10	IRQ7
13	DRQ6	SD10	22	SA9	IRQ6
14	DACK7	SD11	23	SA8	IRQ5
15	DRQ7	SD12	24	SA7	IRQ4
16	+5V	SD13	25	SA6	IRQ3
17	MASTER	SD13	26	SA5	DACK2
18	GND	SD15	27	SA4	TC
19	GND	KEY	28	SA3	BALE
			29	SA2	+5V
			30	SA1	OSC
			31	SA0	GND
			32	GND	GND

2.11. Video output

The EB2410ITX has a flexible video system provided by the LCD controller within the S3C2410 SOC. The signals from the LCD controller are full exposed on PL15 including the ADC channels for the touch screen and power.

Figure 2.10. Video system connections



The Chronitel CH7006 is controlled from the S3C2410 using the I2C bus. The output of the device is routed to a standard

SVGA connector (PL1), the RGB expansion header (PL10) and the SVIDEO port (PL3).

For full details on PL15 the EB2410ITX Connector and link pinouts [<http://www.simtec.co.uk/products/EB2410ITX/files/pinlist.html>] document should be consulted, this contains additional information and comments relevant to using this product.

Chapter 3. Bootloader

3.1. Overview

The Simtec Electronics Advanced Boot Load Environment (ABLE) is a portable modular boot loader for use in applications where an OS must be retrieved and started. ABLE provides extended functionality providing modules for a command line, video consoles, serial consoles, network booting and numerous other facilities.

ABLE is a powerful tool and provides a very flexible environment useful for both development and deployment of systems. ABLE is a boot loader, not an Operating System this distinction can sometimes lead to misunderstandings about the capabilities provided by ABLE. A boot loader in this context is a self contained program which retrieves and starts execution of an Operating System. It does not execute user programs itself (all the CLI commands are built in) and does not provide services to an Operating System once started (PC BIOS perform this role).

The modular nature of ABLE allows the use of the same building blocks for every supported platform. The integration and omission of various modules allow for specific driver sets depending on the peripherals of a platform. The flexibility of this approach allows for a common familiar environment across all supported platforms while still supporting a complete feature set.

This chapter only provides a brief introduction to ABLE. Full documentation can be found in the ABLE user guide [http://www.simtec.co.uk/products/SWABLE/files/able-set/book_userguide.html].

3.2. Getting Started

When a platform is initially powered or a hard reset performed, the ABLE environment will be started and each component module will be loaded in turn. The last module loaded is the ABLE shell, which will present the user with a command line interface.

ABLE has the ability to use a combination of input and output sources to interact with a user. The default is to use all the input and output devices available. For example, on the EB2410ITX both the console serial port and the video display will be used to output and the serial port for input (future versions may support USB keyboards for input).

Example 3.1. Video display after starting ABLE on EB2410ITX

```
selected all-wr for console write stream
selected all-rd for console read stream
DRAM: 128 Mb (134217728 bytes)
BAST: PMU version 1.02, ID 00:01:3d:00:01:6a
ABLE: 2.08 (s3c2410x) (vince@gerald) Fri Apr 8 16:35:26 BST 2005
hdc: TOSHIBA MK1003MAV: ATA PIO mode 4
hdc:Diagnosing disc drive: ok
(hdc) 1GB
(hd0) on ((hdc1):ext2)
(hd1) on (hdc2)
DM9000: dm0: r1, 00:01:3d:00:01:6a int phy, link ok, 100Mbit full duplex
NE2000: ne0: ISA/Generic, 00:01:3d:00:01:6b (EEPROM Invalid / Missing)
TMP101: I2C error (-2)
sys.autoshadow unset, automatically shadowing
>
```

Example 3.2. Serial display after starting ABLE on EB2410ITX

```
SuperIO controller fitted
Initialising
Detecting SDRAM size
SDRAM: BANK6 size 04000000
SDRAM: BANK7 size 04000000
```

```
ABLE: 2.08 (s3c2410x) (vince@gerald) Fri Apr 8 16:35:26 BST 2005
Processor: Samsung S3C2410A (arm920)
System: Machine bast/s3c2410x, Linux id 0x014b
.S3C2410X RTC: 01:46:54, 00/01/2003
NAND: configured boot slot is 0 (card slot)
NAND: found Samsung K9F1208u0a [131072,32,512]
(flash0) on (nand0p1)
(flash1) on ((nand0p2):jffs2)
EEPROM: 24cXX, 1024 bytes, single byte addressed
(nvram0) on (24cxx)
sys.speed is unset, Setting CPU Speed to 266MHz
no configuration, defaulting to VGA
X/Y values invalid, configuring automatically
Chrontel CH7006 detected
screen mode is 640x480, ?Hz, ?Hz HSync
video: video size 300K
configuring ch7006: vga
selected all-wr for console write stream
selected all-rd for console read stream
DRAM: 128 Mb (134217728 bytes)
BAST: PMU version 1.02, ID 00:01:3d:00:01:6a
ABLE: 2.08 (s3c2410x) (vince@gerald) Fri Apr 8 16:35:26 BST 2005
hdc: TOSHIBA MK1003MAV: ATA PIO mode 4
hdc:Diagnosing disc drive: ok
(hdc) 1GB
(hd0) on ((hdc1):ext2)
(hd1) on (hdc2)
DM9000: dm0: r1, 00:01:3d:00:01:6a int phy, link ok, 100Mbit full duplex
NE2000: ne0: ISA/Generic, 00:01:3d:00:01:6b (EEPROM Invalid / Missing)
TMP101: I2C error (-2)
sys.autoshadow unset, automatically shadowing
>
```

The input devices are controlled by using the cons-read parameter and similarly the cons-write parameter controls which output devices are used.

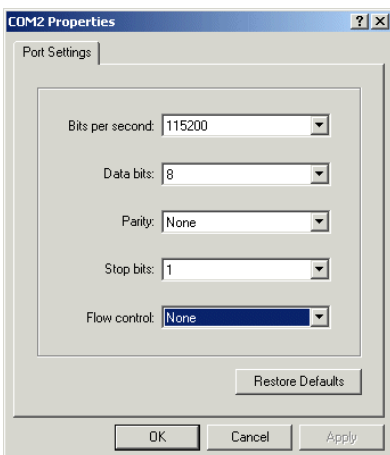
Typically the console serial port is used to interact with the ABLE CLI.

Unless the boot parameters are altered from their default settings the autoboot process will commence. To manually start an Operating System the command line must be used.

3.2.1. Using hyperterm as a serial console

To access the serial console from windows the hyperterm program can be used. Identify which serial port the platform is connected to and ensure a note is made of the correct COM port, e.g. COM1 or COM2.

Figure 3.1. Hyperterm settings window



Start HyperTerminal and create a new connection. When prompted for which modem to use, instead choose the appropriate COM port, as noted earlier. Then the appropriate settings for your platform (please refer to platform specific documentation) typically these settings are 115200 bits per second, 8 data bits, no parity, 1 stop bit and no flow control as shown in Figure 3.1, “Hyperterm settings window”.

Figure 3.2. Hyperterm displaying ABLE output

```

eb675001dip - HyperTerminal
File Edit View Call Transfer Help
Bootswitch configuration 20
oki_eb67dip_bus_init: done
oki_ml67x_init: scanning for OKI_ML67X device
oki_ml67x_scan: bus=00fc7e14, dev=00fc7de4
oki_ml67x: installed routines
EEPROM: 24c8X, 1024 bytes, single byte addressed
(nvram0) on (24c8x)
NVRAM: crc does not match (74 vs ff)
oki_ml67x_timer: registering timers
oki_ml67x_timer: add with irq 1
oki_ml67x_timer_set: twr=00f16d90, scaler=1, period=0x8fff
selected all-wr for console write stream
selected all-rd for console read stream
DRAM: 32 Mb (33554432 bytes)
Ricoh R2051K, 36:21:39, 12hr mode
ABLE: 2.07 (oki-eb67dip,oki-ml67x) (vince@gerald) Wed Feb 23 15:40:22 GMT 2005
(rom0) on (nor0)
SYSTEM: Warning: cannot get unique default MAC
DM9000: dm0: r1, 00:02:04:06:08:0a int phy, link down
failed to find cpu device
boot.cmd unset, defaulting to `(rom1) root=/dev/mtdblock3 ro console=ttyS00,19200`
Autoboot in 12 seconds (attempt 1), Press any key to abort
>
Connected 0/03/01  VT52  115200 8-N-1  SCROLL  CAPS  NUM  Capture  Print extra

```

Once the connection is established the output from ABLE should be seen in the hyperterm window as in Figure 3.2, “Hyperterm displaying ABLE output”

3.2.2. Using minicom as a serial console

To access the serial console from LINUX® the minicom program can be used. Identify which serial port the EB2410ITX is connected to and ensure a note is made of the correct device node, e.g. something like /dev/ttyS0 or /dev/ttyUSB0.

Figure 3.3. Minicom settings window

```

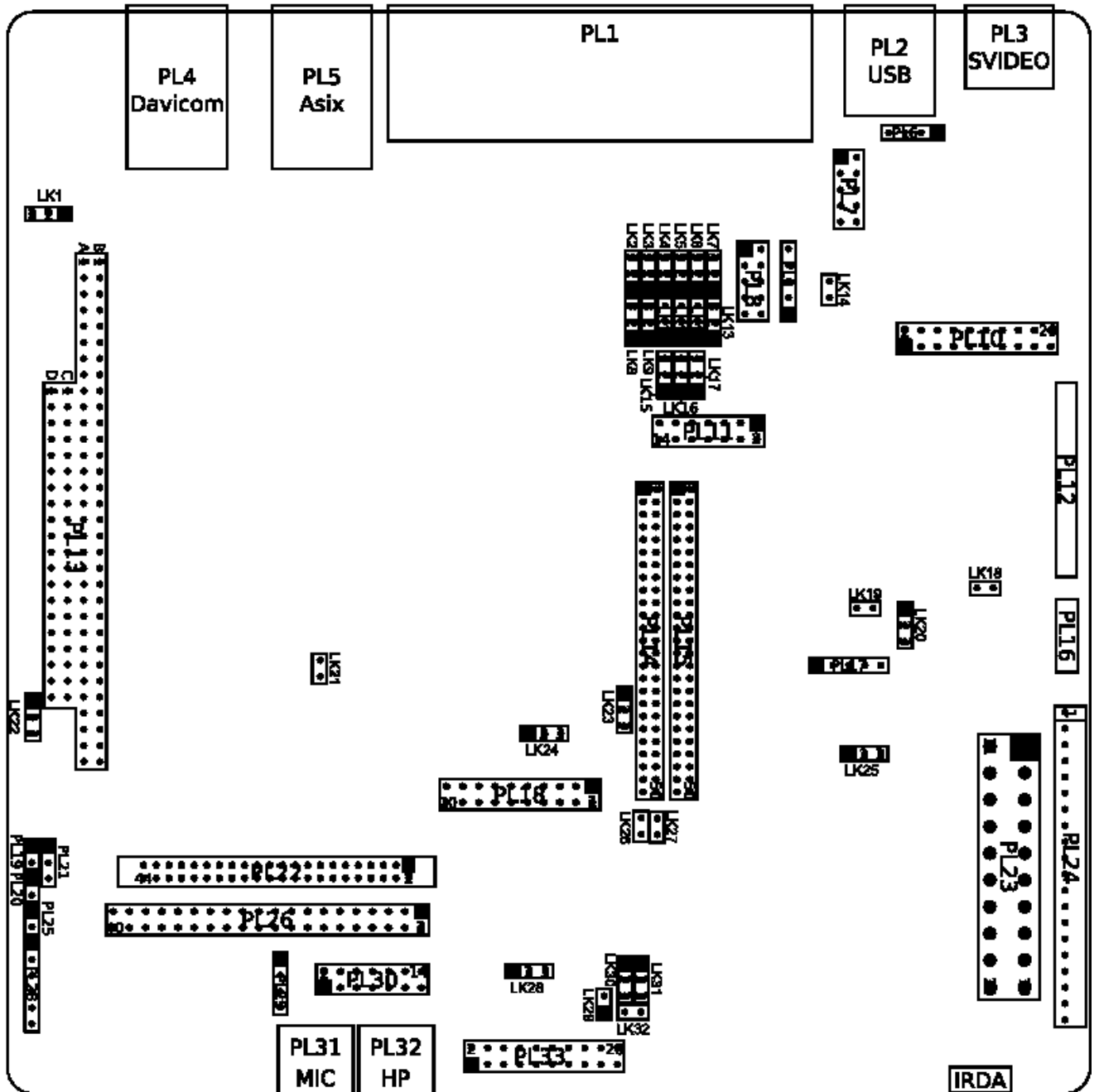
Welcome to minicom 2.1
OPTIONS: History Buf
Compiled on Mar 29 2
Press CTRL-A Z for h
[Comm Parameters]
Current: 115200 8N1
Speed      Parity      Data
A: 300     L: None     S: 5
B: 1200    M: Even     T: 6
C: 2400    N: Odd      U: 7
D: 4800    O: Mark     V: 8
E: 9600    P: Space
F: 19200
G: 38400
H: 57600
I: 115200  Q: 8-N-1
J: 230400  R: 7-E-1
Stopbits
W: 1
X: 2
Choice, or <Enter> to exit?
CTRL-A Z for help | 115200 8N1 | NOR | Minicom 2.1 | VT102 | Offline

```

Start minicom and ensure the correct settings are selected (Default is Ctrl-A p). These settings are 115200 baud, 8 data bits, no parity and 1 stop bit as shown in Figure 3.3, “Minicom settings window”. Obviously Minicom should be using the correct serial port as noted earlier.

Appendix A. Board Layout

Figure A.1. EB2410ITX board connector and link locations



Appendix B. Component Identification

Figure B.1. EB2410ITX top side component identification

