EBSA 21285 Development System
Hardware Description

Introduction

The EBSA-21285 development system is made up of two distinct blocks. The first being the CPU section consisting of a SA110, memory and Footbridge which form a self contained processing system that provides all necessary support for the processor to communicate with memory and devices attached to the PCI bus. The second part is the IO section consisting of a PCI connected 'Southbridge' mega-IO chip to support all the usual PC style IO ports such as parallel, serial, USB, IDE and ISA.

The Processor section

The CPU and memory section consists of the SA-110 processor, the 21285 Footbridge, a byte wide flash memory (2Mbit) and support for up to 256Mb of 50Mhz SDRAM in two sockets. There is also a small amount of level conversion logic used toconvert TTL level clock and Boundary scan signals to LVTTL levels. Although the Footbridge is 5v tolerant (has no clamp to Vcc diodes in its IO pads) the CPU is not.

The CPU

The SA-110 CPU currently shipped is the EA grade part which is rated to 233Mhz with a 50Mhz bus. However the core clock is factory set to 228Mhz via the four resistors R15-17 (R16 is fitted). The core is run from a fixed 2.0v supply generated from the 3.3v rail by the LDO regulator U21.

The Memory

A single byte wide flash memory is used to boot the firmware on reset. For each memory access from the CPU, the Footbridge stalls the CPU clock, performs four sequential byte accesses to the ROM and presents the word of data to the CPU before it is unstalled. A 2Mbit (256K) SST part is shipped as standard, which can be reprogrammed in system by booting a special re-FLASH utility or by invoking a rescue routine from the firmware in case of corruption. As a last resort, the device is socketed to allow for external programming if in-system programming fails and can be replaced by any JEDEC standard 32pin PLCC 3.3v single rail EEPROM or Flash device.

There are several issued that will effect the type of device used:

1) The Footbridge always performs four byte reads from the ROM which prevents out of sequence read operation from being
performed to unprotect some FLASH devices - this prevents the use of SST 4Mbit memories.
2) The 2MBit SST part that is fitted cannot be programmed via the JTAG test port due to timing issues within the device.

Two standard 168pin 3.3v unbuffered SDRAM sockets are provided to take up to 256MB of RAM. Support for SPD (Serial presence detect) is provided by the SMB (serial management bus) on the Southbridge so that device and modules supporting this feature can be interrogated by system software to confirm the presence and type of a module.Due to a limitation of the Footbridge chip, only two physical arrays of memory can be supported, either as one double array module fitted to PL1 or two single array modules in either socket. (The physical arrangement of the modules should not be confused with the internal banking of the SDRAM chips themselves).

Because of these restrictions, we would recommend that only branded single array PC-66 and PC-100 type modules using 64Mbit SDRAM devices be used as this will allow an additional module to be added. We have found that some popular unbranded modules commonly used in PC's, that not conform to the standard, have a different organisation and will not work with the Footbridge. Also, besides differences between manufacturers, there are important differences between PC-66 and PC-100 modules which effect the types of parts that can be fitted. PL1 has all four SDRAM clock lines tracked to the socket to support double array modules, but PL2 has only two clock signals connected (CLK0 and 1) and will only support a single array module.

This was done to prevent damage if two double array modules were accidentally fitted at the same time. Although single array PC-66 modules use CLK0 and 1, PC-100 modules use CLK0 and 2 instead. If a PC-100 module of this type is fitted into PL2, only half the memory contained on the module will be visible. They will work correctly when fitted to PL1.

A PC-100 module can be used in PL2 if it is first modified by using a short piece of wire to link pin 79 of PL1 and PL2 together.

These modules have been tested and are known to work:

Up to two single array modules can be fitted or one dual array module can be fitted.

Manufacturer	Part Number	Array/Module	Capacity	Standard
Samsung	KMM366S104BTN-G0	1	8Mb	PC-66
Samsung	KMM366S203BTN-G2	1	16Mb	
TI	TM4S64EPU-12	2*	32Mb	
Fujitsu	PDC4UV6414B-103TS	1**	32Mb	PC-100
Samsung	KMM366S424BTL-G0	1	32Mb	PC-66
Samsung	KMM366S403CTL-G0	2*	32Mb	PC-66
Samsung	KMM366S823ATL-G0	1	64Mb	PC-66
Fujitsu	PDC8UV8484B-103TS	1**	64Mb	PC-100

*Can only be fitted to PL1 (require SDRAM CLK1-3)
**Needs only two clocks but uses CLK0 and 2, so must be fitted to PL1 or PL2 must be modified.

The Footbridge and PCI bus

All processor, memory, clock and system functions are controlled by the 21285 Footbridge. This co-ordinates all bus transactions between the CPU, memory and the PCI, generating the CPU and SDRAM clocks from a single master clock. The Footbridge also contains a diagnostic serial port which is brought out via a set of links to either the SERIAL2 port (at RS232 levels) or
to the internal IRDA plug PL24 (at TTL levels). The diagnostic port can be used as a terminal for diagnostic output and data input to communicate with the firmware if no keyboard, VGA graphics card or network is attached.

Note: The Serial diagnostic port is set up for 38400 Baud 8N1. Handshaking should be disabled because if LK9-11 are set to route the diagnostic serial port via SERIAL2 only the RX and TX signals are altered, the other control signals are still driven by the Southbridge's COM2 port.

The PCI bus is fully v2.1 compliant, supporting 33Mhz 32bit accesses, with bus arbitration under the control of the Footbridge.Both 5v and 3.3v power is provided, with an option of either 5v or 3.3v IO signalling which is currently factory set for 5v. The only signal not supported is the PCI #Lock signal for locked PCI cycles. Although the optional presence detect is not supported, PMJ power management signalling is bussed to each PCI socket and routed to a pin on the Southbridge (DOCK).

Besides the internal timers, all external interrupts are processed via the Footbridge. Unlike the Digital EBSA evaluation board, the fixed 3.68Mhz clock is not fed into the Footbridge's IRQ INT2 pin (for memory clock independent timing), but used instead to route the unified Southbridge system interrupt. If system timers are required to be independent of the main memory clock (FCLK) then the PC style ISA timers are available in the southbridge, which are clocked from a fixed 14.318Mhz source.The PCI interrupts are routed in the same way as the Digital EBSA board, with INTA-D routed to PCI_IRQ, IRQ_INT0 ,1 and 3.These signals are pulled high to VIO by 10K resistors.

Test points:

Number	Name	Function	level	type
TP5	nMREQ	memory request from processor	LVTTL	O
TP6	REQ/GNT	Footbridge PCI request signal	VIO	O
TP9	nR/W	CPU read/write pin	LVTTL	O
TP11*	MCLK	CPU memory clock	LVTTL	O
TP12	3.6MOSC5	CPU PLL reference clock (before level shifting)	TTL	O
TP13	P_RST	Processor/Footbridge reset (active low)	LVTTL	OD
TP14	RST_OUT	CPU reset out (active low while in reset or core PLL not locked)	LVTTL	O

*Do not apply excessive load to signal while monitoring

User configurable links:

It is advisable to read this along side the Footbridge TRM for a detailed explanations of the function of each configuration option and their effects on the system.

Number	Function	Link Settings	
LK7	Central function (PCI_CNF)	1-2 : Master	2-3 : Slave
LK12	Set Output hold times (MA2 config.)	1-2 : Extended	2-3 : Normal
LK13	Set Input hold times (MA3 config.)	1-2 : Extended	2-3 : Normal
LK14	Blank ROM setting (MA6 config.)	1-2 : Blank	2-3 : Normal

Manufacturing resistor options:

Several configuration options have been set during manufacture and are not intended to be user modified and are provided for information only.

Component	Name	Function
R15	CCCFG<3>	When fitted, the 22R resistors pull the selected CCCFG pin low
R16	CCCFG<2> *Fitted	With CCFG<3..1> set to 1101 this equates to a cache clock of 228.1Mhz
R17	CCCFG<1>	using a 3.68Mhz reference clock
R18	CCCFG<0>	
R135	Alternate VCO table	When fitted, enable the alternate VCO divider table on future processors.

JTAG connector : PL18

The JTAG socket can be used for remote debugging of the system and ISP of the Flash memory (see section on FLASH memory restrictions). All inputs are level shifted and clamped and can accept signals in the range -1 to +6v. The boundary scan chain TDI pin, after conditioning, feeds first to the CPU, and then from the CPU TDO to the TDI pin of the Footbridge. The Footbridge TDO is then buffered and wired back to the connector. Below is the pinout of the JTAG connector PL18:

Pin	Name	Function	
1, 13	VCC	5v power for cable buffer protected by a 22R series resistor	
3	TRST	boundary scan reset pin	(10k pull down to GND)
5	TDI	TDI	(10k pull down to GND)
7	TMS	TMS	(10k pull down to GND)
9	TCK	TCK	(10k pull down to GND)
11	TDO	TDO buffered output	(LVTTL)
12	RST	System reset (Open collector)	(10K pull up to 5v)
2, 6, 8, 10, 14	GND		

Southbridge "Mega IO" and ISA bridge

All key IO is provided by the M1543C PCI to ISA Southbridge from Acer Labs. Besides the main function of generating a full ISA bus with master and DMA capability, it also hosts all of the other IO of the system. It provides two independent bus mastering IDE channels, two USB ports, keyboard, mouse, SMB (I2C), IRDA, floppy, parallel, and two serial ports. For a full explanation of the Southbridge's features and register map, consult the M1543 data sheet.

The Southbridge provides a conventional PC compliant ISA bus and IO, which we have endeavoured to follow as close as possible to the standard. There are some important differences, which are necessary due to the difference in processor and will be described below:

Interrupt structure.

As mentioned in the Footbridge section, the four PCI interrupts INTA..D are routed directly to the Footbridge along with a single Southbridge interrupt (the INTR pin) combining all ISA and southbridge interrupts. The PCI interrupts are routed to the southbridge as they would be in a PC and can be assigned ISA interrupts, but their direct connection to the Footbridge allows more flexibility in IRQ/FIQ routing than would be available in the southbridge alone and leaves more ISA interrupt signals free for expansion cards and peripherals.

IRQ mapping

IRQ	Function
0	ISA Timers 0,1 and 2
1	PS2 Keyboard
2	Cascade input from second IRQ controller (INT8..15)
3	COM1
4	COM0
5	*unallocated
6	Floppy controller
7	Printer
8	RTC alarm
9	*unallocated
10	*unallocated
11	USB controller
12	PS2 Mouse
13	FP error - SMI interrupt connected to this point
14	Primary IDE channel
15	Secondary IDE channel

*unallocated interrupts are not assigned by the firmware.

SMI interrupts:

Because the ARM processor has no support for system management interrupts, the SMI IRQ is connected to the otherwise unused floating point unit error pin (IRQ13). This allows routing of system management IRQ's via ISA to the Footbridge. The active low SMI signal is linked directly to the nFERR/IRQ13 pin on the southbridge. This interrupt can be monitored from test point TP17.

DMA channels:

Out of the eight DMA channels available, the 8 bit DMA channels 2 and 4 are used for floppy and cascade. Channels 0,1 and 3 are unallocated as are the 16 bit channels 5,6 and 7.

One wire Bus and I2C connector : PL15

The connector allows off board control of IIC bus peripherals using the southbridge's SMB controller. All IO signal levels are LVTTL. Below is the pinout of the OWB/IIC connector PL15

Pin	Function	Comments
1	One wire bus (SD4/GPIO4)	4K7 pull-up to 5v
2	GND	
3	I2C Data (LVTTL)	4K7 pull-up to 3.3v
4	I2C Clock (LVTTL)	4K7 pull-up to 3.3v
5	GND	

SQW/SPLED LED control:

There are two LED outputs which are controlled by the southbridges SQW and SPLED outputs. The SPLED is powered by the 5v SBY supply and will light when the system is off.

SQW LED : LK3

PIN	Function
1	+ve 5v supply with 180R series resistor
2	-ve inverting logic (74AC14) with 110R series resistor

SPLED LED : LK2

PIN	Function
1	+ve 5v supply with 180R series resistor
2	-ve inverting logic (74AC14) with 110R series resistor

IDE Disk drive activity LED : LK1

PIN	Function
1	+ve 5v supply with protective series resistor
2	-ve drain signal from IDE drive (diode ORed and resistively damped)

Power LED and Keyboard lock : PL13

PL13 provides power for the power on LED and input pins for a keyboard lock switch. The LED pins will directly drive an LED which illuminates at half intensity when the system is in standby mode (Power supply on but system power inactive) to give a visual indication of the system state. The keyboard lock will block any keyboard input. These pins are left open for normal operation but the keyboard can be locked if the pin is pulled low.

PIN	Function
1	+ve 5v supply (1K pull up to 5v in parallel with a 390R pull up to 5v standby supply)
2	nc
3	GND
4	KEYLOCK (4K7 pull up to 5v)
5	GND

RESET button : LK15

When the RESET pin is pulled low with a n.o. non-latching pushbutton switch, the system will be reset. The system reset line
will be held active for at least 150ms after the reset button is released.

PIN	Function
1	PUSHBUTTON RESET (10K pullup to 5v)
2	GND

POWER BUTTON INPUT : LK15

This is a debounced active low input that activates the 'suspend and resume' logic within the Southbridge to enable the PSU to turn on system power. If momentarily pulled low, the system will toggle between power on and soft suspend mode. If held forfour seconds, the resume circuit will disable the PSU output and so turn off system power. The exact behaviour can be modifiedby system software by configuring the Southbridge to either generate an event or power off immediately.

PIN	Function
1	POWER BUTTON (10K pullup to 5v standby)
2	GND

PC beeper SPEAKER connection : PL20

This header will drive a standard 8 Ohm PC speaker from the buffered square wave PC beep output.

PIN	Function
1	-ve beep output (active low open collector)
2	nc
3	GND
4	5v (unfused)

RTC clear and external Battery feed : PL21

To enable the clearing of CMOS RAM to default settings, the link cap on PL21 should be momentarily moved to position 3-4.By default, the link cap is parked on pins 2 and 3. To prolong the life of the RTC's internal lithium battery of the RTC or should it become exhausted, the link cap is removed and an external 3v supply connected between pins 1 (+ve) and 4 (-ve).

PIN	Function
1	+ve 3v auxiliary battery input (2.5v to 4.5v)
2	nc
3	RAM CLEAR
4	GND

Wake up connector : LK19

The wake up header allows access to the RTC low asserted KS pin to wake up the system. This can be routed through the RTC to generate an alarm on INT8.

PIN	Function	Comments
1	5v supply	
2	active low Wake up to RTC (KS)	10K pull-up to 5v SBY
3	GND	

Ring Indicate : LK16

When fitted, any ring signal present on the RI pin of the Serial1 connector will activate the RI_RSM pin on the Southbridge. If the appropriate Southbridge 'suspend and resume' registers are set then the system will power up when this signal goes active. The system will continue to be active until both the ring signal is removed and the wake up condition is cleared.

POWER mode selection : LK18

The power link should be left in position 1-2, where the southbridge OFF_POWER_2 pin controls the output of the ATX power supply. If instant power on is required, contact Chalice for resistor mods required for the pcb. Although the PSU can be hard wired on by changing to position 2-3, the southbridge still needs to be 'woken up' for correct system operation.

ATX POWER feed : PL23

Power is supplied to the motherboard via a MOLEX5566-N20 2x10 pin latching connector. A standard ATX power supply that generates 3.3v and supports PSU output disable can be used. Care should be taken in choosing a PSU to ensure that its outputs remain stable under light load conditions if only the motherboard is to be powered.

The ATX power connector has the following pinout

PIN	**Function**
1,2,11	+3.3v
4,6,19,20	+5v
10	+12v
12	-12v
18	-5v (routed to ISA slots only - not used by motherboard)
3,5,7,13,15,16,17	GND
8	DC_OK (Output form PSU to notify stable supply - not used on current motherboards)
9	+5v standby supply (to power the 'suspend and resume' cct for soft PSU control)
14	PSU_ENABLE (driven low by the motherboard, the PSU is enabled - 4/4mA drive)

Serial port routing options:

By default, the board is shipped with the Southbridge's Serial1 routed permanently to COM1 and either the Footbridge's diagnostic port or Southbridge's Serial2 routed to COM2 according to the setting of links LK8 and LK10. Associated with these are LK9 and LK11 which route the unrouted TTL level serial signals to the IRDA connector. Care should be taken when routing signals to prevent both IRDA and COM2 being driven from the same source. The Footbridge serial interface can be operated in either standard mode or IRDA mode by setting the appropriate Footbridge registers. The Southbridge uses a dedicated set of pins separate from the normal Serial2 lines for IRDA. It is possible to route the Southbridge Serial2 to COM2, and the IRRX/IRTX pins to the IRDA connector. With the M1543 rev C, a third serial port can be used for IRDA use, allowing both serial ports (Serial1 and Serial2) to be used simultaneously. In earlier versions, Serial2 is shared and requires the appropriate port to be selected using the internal port selector registers in the Southbridge.

Serial port routing	**LK8**	**LK10**
Footbridge Serial to COM2	2-3	2-3
Southbridge Serial2 to COM2	1-2	1-2

IRDA port routing	**LK9**	**LK11**
Footbridge Serial to IRDA	1-2	1-2
Southbridge IRDA pins	2-3	2-3

IRDA connector PL24:

PIN	**Function**	**Comment**	**level**
1	Filtered 5v power		
2	FIR(SD1/GPIO1)	Select fast IR mode	TTL
3	IR_RX(from LK11)	input from IR receiver	TTL

4	GND		
5	IR_TX(from LK9)	output to IR transmitter	TTL
6	IR_OFF(SD3/GPIO3)	output to disable IR module	TTL

Test points:

Number	Name	Function	level	type
TP1	PCI_CLK	unused PCI clock (CPU_CLK/2)	TTL	O
TP2,4	CPU_CLK	unused CPU_CLK set by LK4,5	TTL	O
TP15	DC_OK	active when PSU output are stable	TTL	O
TP17	nSMI/IRQ13	feedback of SMI interrupt to IRQ13 input (Southbridge)	LVTTL	O
TP16	SER_IRQ	PCI Serialized IRQ/GPI12 (4K7 pull up to 5v) (Southbridge)	TTL	I
TP7	GPO18	BIOSA16/GPO18 output (Southbridge)	LVTTL	O
TP10	GPO19	BIOSA17/GPO19 output (Southbridge)	LVTTL	O